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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/632,653	08/02/2003	Robert M. Geffken	BUR9-2000-0063-US2	3573

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SCHMEISER, OLSEN + WATTS
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EXAMINER	
PERKINS, PAMELA E	

ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 11/17/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/632,653	GEFFKEN ET AL.	
	Examiner	Art Unit	
	Pamela E Perkins	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 August 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *15-40* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *15-20, 22, 24-31, 34 and 38-40* is/are rejected.

7)☒ Claim(s) *21,23,32,33 and 35-37* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 August 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *8/2/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This office action is in response to the filing of the application papers on 2August 2003. Claims 15-40 are pending.

Drawings

Figures 1-3E should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.121(d)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference character(s) not mentioned in the description: reference number 16, see figure 1. Corrected drawing sheets in compliance with 37 CFR 1.121(d), or amendment to the specification to add the reference character(s) in the description in compliance with 37 CFR 1.121(b) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as

per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 15-18, 20, 22, 24-31, 34 and 38-40 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's prior art in view of Joshi et al. (6,323,554) and Zhou et al. (6,376,353).

Applicant's prior art discloses a method for forming an electronic structure where a substrate layer (12) that includes a first electronic device (20); forming a passivating layer (48) on the substrate layer (12) and in mechanical contact with the substrate layer (12), wherein the passivating layer (48) is on the first electronic device (20) and is in mechanical contact with the first electronic device (20); forming a first insulative layer (14) on the passivating layer (48) and in mechanical contact with the passivating laver (48) (Fig. 1; page 1); forming a first damascene conductive wire/stud (61) in the first insulative layer (14); forming a second damascene conductive wire/stud (62) in the first insulative layer (14) such that a lower portion of the second damascene conductive

wire/stud (62) is conductively coupled to a second portion of the first electronic device (20) (Fig. 3A; pages 2-4); forming a second insulative layer (8) on the first insulative layer (14); and forming a damascene conductive wiring line structure (3) within the second insulative layer (8). Applicant's prior art further discloses the substrate layer (12) further comprising a second electronic device (30), and wherein forming the electronic structure further comprises forming a second damascene conductive wire/stud (63) in the first insulative layer (14) such that a lower portion of the second damascene conductive wire/stud (63) is conductively coupled to a portion of the second electronic device (30) (Fig. 3A; page 3 & 4); and forming a damascene conductive wiring line (5) within the second insulative layer (8), wherein the damascene conductive wiling line (5) is above the second damascene conductive wire/stud (63) and is insulatively isolated from the second damascene conductive wire/stud (63) (Fig. 3B; page 4 & 5).

Claim 16, Applicant's prior art discloses the step of forming a first damascene conductive wire/stud (61) includes conductively coupling a lower portion of the first damascene conductive wire/stud (61) to a first portion of the first electronic device (20) (pages 3 &4).

Claim 18, Applicant's prior art disclose the first electronic device (20) is a field effect transistor (FET), wherein the first portion of the first electronic device (20) includes a gate of the FET, and wherein the second portion of the first electronic device (20 is selected from the group consisting of a source of the FET and a drain of the FET (21, 22) (page 1).

Claim 22, Applicant's prior art disclose the substrate (12) includes a shallow trench isolation (STI) (46), and wherein the step of forming a first damascene conductive wire/stud (70) includes forming a lower portion of the first damascene conductive wire/stud (70) on the STI (46) (Fig. 3E; page 7).

Claim 26, Applicant's prior art disclose the first damascene conductive wire/stud (61) includes an internal seam or void (71) oriented lengthwise within the first damascene conductive wire/stud (61) (Fig. 3A; pages 3 & 4).

Claim 34, Applicant's prior art disclose the damascene conductive wiring line structure (3) comprises a damascene conductive wiring line (3) and a conductive liner (130) formed on sides of the damascene conductive wiring line (3) (Fig. 3B; pages 4 & 5).

Claim 38, Applicant's prior art disclose the passivating layer (48) comprising a material selected from the group consisting of silicon nitride and silicon carbide (pages 1 & 2).

Claim 39, Applicant's prior art disclose the first insulation layer comprises a material selected from the group consisting of phososilicate glass and borophososilicate glass (pages 1 & 2).

Applicant's prior art do not disclose removing a top portion of the first insulative layer such that an upper portion of the first damascene conductive wire/stud is above the first insulative layer after the moving; forming a metallic capping layer on the first insulative layer such that the metallic capping layer is in conductive contact with the first damascene conductive wire/stud; subtractively etching a portion of the metallic capping layer to form a subtractive etch metallic cap on the upper portion of the first damascene

conductive wire/stud such that the subtractive etch metallic cap is in conductive contact with the first damascene conductive wire/stud.

Joshi et al. disclose a method for forming an electronic structure where a substrate layer (10) that includes a first electronic device (18); forming a first insulative layer (20) on the first electronic device (18) and substrate layer (10) (Fig. 3B); forming a first damascene conductive wire/stud (16/17) in the first insulative layer (15) (Fig. 4C; col. 8, lines 28-54); removing a top portion of the first insulative layer (15) such that an upper portion of the first damascene conductive wire/stud (16/17) is above the first insulative layer (15) after the removing (Fig. 4D; col. 8, lines 28-54); forming a second insulative layer on the first insulative layer; and forming a damascene conductive wiring line structure within the second insulative layer (Fig. 8; col. 11, lines 57-65).

Since Applicant's prior art and Joshi et al. are both from the same field of endeavor, a method for forming an electronic structure, the purpose disclosed by Joshi et al. would have been recognized in the pertinent art of Applicant's prior art. Therefore, it would have been obvious to one ordinary skill in the art at the time the invention was made to modify Applicant's prior art by removing a top portion of the first insulative layer such that an upper portion of the first damascene conductive wire/stud is above the first insulative layer after the moving as taught by Joshi et al. to prevent corrosion (col. 3, lines 31-63).

Referring to claim 30, Joshi et al. do not disclose the distance between a top surface of the first damascene conductive wire/stud and a top surface of the first insulative layer is between about 100 nm and about 400 nm. It would have been

obvious to one having ordinary skill in the art at the time invention was made to have the distance between a top surface of the first damascene conductive wire/stud and a top surface of the first insulative layer is between about 100 nm and about 400 nm disclosed in the claimed invention, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller*, 105 USPQ 233 (CCPA 1955).

Zhou et al. disclose a method for forming an electronic structure where a substrate layer (1) that includes a first electronic device; forming a passivating layer (12) on the substrate layer (1) and in mechanical contact with the substrate layer (1); forming a first insulative layer (14/16) on the passivating layer (12) and in mechanical contact with the passivating laver (12); forming a first damascene conductive wire/stud (24) in the first insulative layer (14/16); forming a metallic capping layer (25) on the first insulative layer (14/16) such that the metallic capping layer (25) is in conductive contact with the first damascene conductive wire/stud (24) (Fig. 3c; col. 8, lines 10-27); subtractively etching a portion of the metallic capping layer (25) to form a subtractive etch metallic cap on the upper portion of the first damascene conductive wire/stud (24) such that the subtractive etch metallic cap is in conductive contact with the first damascene conductive wire/stud (25) (Fig. 3d; col. 8, lines 28-40).

Claim 24, Zhou et al. disclose the metallic capping layer has a thickness between about 20 to 5000 Angstroms[1] (col. 8, lines 19-22).

[1] 20 Angstroms = 2nm

Claims 25 and 29, Zhou et al. disclose the metallic capping layer includes an electrically conductive material selected from the group consisting of tantalum, titanium nitride, tantalum nitride and tungsten nitride (col. 8, lines 19-25).

Claim 27, Zhou et al. disclose the subtractively etching step includes selective etching of the portion of the metallic capping layer (25) with respect to the first damascene conductive wire/stud (24), wherein the metallic capping layer (25) includes a first electrically conductive material, and wherein the first damascene conductive wire/stud (24) includes a second electrically conductive material which differs from the first electrically conductive material (col. 7, line 56 thru col. 8, line 25).

Claim 28, Zhou et al. disclose the first electrically conductive material is selected from the group consisting of tantalum, titanium nitride, tantalum nitride and tungsten nitride, and the second electrically conductive material is elected from the group consisting of copper (col. 7, line 56 thru col. 8, line 25).

Since Applicant's prior art and Zhou et al. are both from the same field of endeavor, a method for forming an electronic structure, the purpose disclosed by Zhou et al. would have been recognized in the pertinent art of Applicant's prior art. Therefore, it would have been obvious to one ordinary skill in the art at the time the invention was made to modify Applicant's prior art by forming a metallic capping layer on the first insulative layer such that the metallic capping layer is in conductive contact with the first damascene conductive wire/stud; subtractively etching a portion of the metallic capping layer to form a subtractive etch metallic cap on the upper portion of the first damascene conductive wire/stud such that the subtractive etch metallic cap is in conductive contact

with the first damascene conductive wire/stud as taught by Zhou et al. to prevent peeling (col. 3, lines 9-15).

Referring to claims 31 and 40, Applicant's prior art in view of Joshi et al. and Zhou et al. do not disclose the first insulative layer has a thickness between about 0.2 microns and about 1.5 microns. It would have been obvious to one having ordinary skill in the art at the time invention was made to have the first insulative layer has a thickness between about 0.2 microns and about 1.5 microns disclosed in the claimed invention, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller*, 105 USPQ 233 (CCPA 1955).

Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's prior art in view of Joshi et al. and Zhou et al. as applied to claim 15 above, and further in view of Adler et al. (6,259,128).

Applicant's prior art in view of Joshi et al. and Zhou et al. disclose the subject matter claimed above except the first electronic device is selected from the group consisting of an MOS capacitor, a resistor, an inductor, a, charged coupled device, and a light emitting diode.

Adler et al. disclose a method for forming an electronic structure where a substrate layer (10) that includes a first electronic device (100); forming a passivating layer (120) on the substrate layer (10), wherein the passivating layer (120) is on the first electronic device (100) and is in mechanical contact with the first electronic device (100); forming a first insulative layer (130) on the passivating layer (120) and in

mechanical contact with the passivating laver (120); forming a first damascene conductive wire/stud (150) in the first insulative layer (130) (Fig. 3A; col. 33-48). Adler et al. further disclose the first electronic device as an MOS capacitor (col. 3, lines 42-48).

Since Applicant's prior art and Adler et al. are both from the same field of endeavor, a method for forming an electronic structure, the purpose disclosed by Adler et al. would have been recognized in the pertinent art of Applicant's prior art. Therefore, it would have been obvious to one ordinary skill in the art at the time the invention was made to modify Applicant's prior art by forming the first electronic device as an MOS capacitor as taught by Adler et al. for better conductivity and electromigration resistance (col. 1, lines 32-56).

Allowable Subject Matter

Claims 21, 23, 32, 33 and 35-37 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter: prior art does not anticipate, teach, or suggest subtractively etching away all conductive material of the metallic capping layer that had been in conductive contact with the second damascene conductive wire/stud; forming a second subtractive etch metallic cap on the first insulative layer such that the second subtractive etch metallic cap is insulatively isolated, and further comprising forming a dual damascene within the

second insulative layer such that the dual damascene is above the second subtractive etch metallic cap and is conductively coupled to the second subtractive etch metallic cap; a passivating film disposed between the first insulative layer and the second insulative layer; and/or the damascene conductive wiring line structure together with the subtractive etch mechanical cap and the first damascene conductive wire/stud are adapted to collectively couple the first electronic device to other conductive structure in interlevel dielectric layers which are at or above the damascene conductive wiring line structure.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Pamela E Perkins whose telephone number is (571) 272-1840. The examiner can normally be reached on Monday thru Friday, 9:00am to 5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on (571) 272-1852. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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